

DECIMAL MULTIPLICATION USING DIGIT RECODING

ABSTRACT OF THE DISCLOSURE

A system and methodology for decimal multiplication in a microprocessor comprising: a recoder configured to recode decimal digits of a first operand to a corresponding set of $\{-5 \text{ to } +5\}$. The recoder also configured to recode decimal digits of a second operand to a corresponding set of $\{-5 \text{ to } +5\}$. The system also includes a multiplier array of digit multipliers, each digit multiplier configured to generate a partial product of a selected digit of a recoded first operand and a recoded second operand; and an adder array of digit adders, each adder configured to generate a sum of the partial products, wherein a least significant digit of the sum is shifted to a results register, and each adder includes carry feedback.